

## WHAT IS CLAIMED IS:

1. A tape for chip on film on which a semiconductor element is mounted and resin is applied for sealing the semiconductor element, the tape for chip on film

5 comprising:

an insulating tape;

a plurality of wiring patterns formed on the insulating tape;

10 a solder resist partially covering the wiring patterns by application to have an opening; and

15 a dummy pattern provided at a corner of a region for the semiconductor element to be mounted so as to control flow of the resin from the corner to a space between a surface of the semiconductor element and the insulating tape during resin sealing.

2. The tape for chip on film as defined in Claim 1, wherein

the dummy pattern is provided independent of the wiring patterns and the solder resist.

20 3. The tape for chip on film as defined in Claim 2, wherein

25 the dummy pattern is provided inside the opening of the solder resist and inside or outside the corner, and a shape of the dummy pattern is formed along a shape of the corner.

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4. The tape for chip on film as defined in Claim 2,  
wherein

the dummy pattern is provided inside the opening  
of the solder resist and extended from outside to inside  
5 the corner.

5. The tape for chip on film as defined in Claim 2,  
wherein

the dummy pattern is provided from outside or  
inside the corner to the solder resist.

10 6. The tape for chip on film as defined in Claim 1,  
wherein

the dummy pattern is composed of a large width  
section of an inner lead of a wiring pattern inside the  
opening of the solder resist.

15 7. The tape for chip on film as defined in Claim 1,  
wherein

the dummy pattern is provided at least at two  
adjacent corners of the region for the semiconductor  
element to be mounted.

20 8. The tape for chip on film as defined in Claim 1,  
wherein

material and thickness of the dummy pattern is  
the same as those of the inner lead.

9. A tape for chip on film on which a semiconductor  
25 element is mounted and resin is applied for sealing the

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semiconductor element, the tape for chip on film comprising:

an insulating tape;

5 a plurality of wiring patterns formed on the insulating tape; and

a solder resist partially covering the wiring patterns by application to have an opening, wherein

10 an opening edge of the solder resist opposed to a corner of a region for the semiconductor element to be mounted is located in a vicinity of the corner, and a shape of the opening edge of the solder resist in the vicinity of the corner is made along a shape of the corner so as to control flow of resin from the corner to a space between a surface of the semiconductor element and the insulating tape during resin sealing.

10. A tape for chip on film on which a semiconductor element is mounted and resin is applied for sealing the semiconductor element, the tape for chip on film comprising:

20 an insulating tape;

a plurality of wiring patterns formed on the insulating tape;

a solder resist partially covering the wiring patterns by application to have an opening; and

25 an inner lead in a wiring pattern located on a

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specified side of a region for the semiconductor element to be mounted inside the opening of the solder resist, wherein

the inner lead has a large width section wider than an electric connection section of the inner lead connected to the semiconductor element so as to control flow of resin from the specified side to a space between a surface of the semiconductor element and the insulating tape during resin sealing.

11. The tape for chip on film as defined in Claim 10, wherein

the large width section of the inner lead is disposed either outside or inside a border line of the region for the semiconductor element to be mounted, or from outside to inside the border line of the region.

12. The tape for chip on film as defined in Claim 10, wherein

the large width section of the inner lead is disposed from outside or inside a border line of the region for the semiconductor element to be mounted to inside a region for the solder resist to be applied.

13. The tape for chip on film as defined in Claim 10, further comprising:

a dummy pattern provided at a corner of a region for the semiconductor element to be mounted so as to control flow of the resin from the corner to a space

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between a surface of the semiconductor element and the insulating tape during resin sealing.

14. The tape for chip on film as defined in Claim 10, wherein

5 an opening edge of the solder resist opposed to a corner of a region for the semiconductor element to be mounted is located in a vicinity of the corner, and a shape of the opening edge of the solder resist in the vicinity of the corner is made along a shape of the corner so as to  
10 control flow of resin from the corner to a space between a surface of the semiconductor element and the insulating tape during resin sealing.

15. The tape for chip on film as defined in Claim 9, further comprising:

15 a dummy pattern provided at a corner of a region for the semiconductor element to be mounted so as to control flow of the resin from the corner to a space between a surface of the semiconductor element and the insulating tape during resin sealing.

20 16. The tape for chip on film as defined in Claim 13, wherein

the wiring pattern, the inner lead, and the dummy pattern are fixed to the insulating tape without use of an adhesive.

25 17. The tape for chip on film as defined in Claim 13,

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wherein

the wiring pattern, the inner lead, and the dummy pattern are fixed to the insulating tape with use of an adhesive.

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18. A semiconductor device comprising a semiconductor element mounted on the tape for chip on film as defined in any one of Claims 1 to 17 and sealed with resin.

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